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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,383	10/25/2005	Hendrikus Petrus Elisabeth Vranken	NL 030461	7931

65913 7590 01/25/2008

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EXAMINER	
MCMAHON, DANIEL F	

ART UNIT	PAPER NUMBER
4146	

NOTIFICATION DATE	DELIVERY MODE
01/25/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/554,383	VRANKEN ET AL.	
	Examiner	Art Unit	
	DANIEL F. MCMAHON	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 October 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/554383, filed on 10/25/2008.

Drawings

The drawings are objected to because of the following formalities:

1. Figure 1A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

2. Figure 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

3. Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is too general.

5. The application appears to be in International form, Standard US format is required (37 CFR 1.77).

Appropriate correction is required.

6. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant's language is convoluted and unclear. At present, a prior art search can not be conducted.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 8-10, and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Venkataraman et al. (herein Venkataraman), "An Efficient Bist Scheme Based On Reseeding Of Multiple Polynomial Linear Feedback Shift Register".

9. With regard to claim 1, Venkataraman discloses: A method of compressing data comprising a sequence of at least two subsequent vectors (page 574, Compaction of Testcubes); wherein a vector comprises one or more bits, the method being characterized by the steps of: (i) comparing corresponding bits of two or more subsequent vectors to determine if they are compatible; and, if all corresponding bits of said vectors are compatible; (ii) merging said two or more vectors to create a single vector representative thereof; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values (page 574, Compaction of Testcubes).

10. With regard to claim 2, Venkataraman discloses: data comprising test vector data for use in testing a logic product, and the method includes the steps of generating or obtaining original test vector data comprising "care" bits and "don't care bits", and compressing said test vector data according to steps (i) and (ii) (page 574, Compaction of Testcubes).

11. With regard to claim 3, Venkataraman discloses: original test vector data is generated by means of an Automated Test Pattern Generation (ATPG) tool (page 572, paragraph 5).

12. With regard to claim 8, Venkataraman discloses: an apparatus for compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by: (i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and (ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values (page 574, Compaction of Testcubes).

13. With regard to claim 9, Venkataraman discloses: data comprising test vector data for use in testing a logic product (page 573, paragraph 2), and the apparatus includes means for generating or receiving original test vector data comprising a sequence of two or more vectors (figure 1), wherein a vector comprises one or more bits, including "care" bits and "don't care" bits (page 574, Compaction of Testcubes).

14. With regard to claim 10, Venkataraman discloses: means for generating original test vector data, apparatus for compressing said original test vector data according to claim 9, means for reconstructing said test data from said compressed data, means for applying said reconstructed data to an input of said logic product, and means for obtaining the resultant output data (figure 1).

15. With regard to claim 13, Venkataraman discloses: an apparatus according to claim 10, wherein said means for generating original test vector data comprises an Automated Test Pattern Generation (ATPG) tool (page 572, paragraph 5).

16. With regard to claim 14, Venkataraman discloses: means for reordering a test pattern, prior to compression (page 574, Compaction of Testcubes).

17. With regard to claim 15, Venkataraman discloses: means for storing merged data sequences in the form of a data set for use in testing a logic product (figure 1).

18. With regard to claim 16, Venkataraman discloses: Electronic data storage means on which is stored a data set created by means of apparatus according to claim 15 (figure 1; page 573, paragraph 3).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman as applied to claim 1 above, and in view of Distler et al. (herein Distler), U.S. Publication 2002/0099992.

20. With regard to claim 4, Venkataraman teaches all the limitations of claim 1, as cited above. Venkataraman does not teach: generating a repeat value in respect of one or more merged vectors, said repeat value being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative.

Distler teaches: generating a repeat value in respect of one or more merged vectors, said repeat value being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative (paragraph 0026).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman: compressing data comprising a

sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by (i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and (ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values; with the teaching of Distler: generating a repeat value; for the purpose of increasing fault coverage of the compressed vector during test.

21. With regard to claim 5, Venkataraman and Distler teach all limitations of claim 4, as cited above. Additionally, Venkataraman teaches: a data set comprising test vector data for use in testing a logic product (page 573, paragraph 2).

22. With regard to claim 6, Venkataraman and Distler teach all limitations of claim 5, as cited above. Venkataraman does not teach: reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data.

Distler teaches: reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data (paragraph 0026).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman, as cited above for claim 1, 4, and 5; with the teaching of Distler: reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data; for the purpose of increasing fault coverage of the compressed vector during test.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman and Distler as applied to claim 6 above, and further in view of Wang, Chiou, (herein Wang), "Generating Efficent Tests for Continious Scan".

23. With regards to claim 7, Venkataraman and Distler teach all the limitations of claim 6, as cited above, compressing two vectors, generating a repeat value, and reconstructing the compressed vectors. Venkataraman and Distler do not teach: compressing said output data. Wang does teach: compressing said output data (page 162, column 2, lines 10-11).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman and Distler: compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by (i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are

compatible; and (ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values; generating a repeate vaule; with the teaching of Wang: compressing said output data, for the purpose of reducing the number of clock cycles required to scan out test results (Wang, page 162, column 2, lines 13-16).

Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman as applied to claim 10 above, in view of Wang.

24. With regard to claim 12, Venkataraman teaches all the limitations of claim 10, as cited above. Additionally, Venkataraman teaches: an apparatus according to claim 10, for compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by (i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and (ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values (page 574, Compaction of Testcubes). Venkataraman does not teach: compressing said output data. Wang teaches: compressing said output data (page 162, column 2, lines 10-11).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman: compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by (i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and (ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically incompatible or opposite values; with the teaching of Wang: compressing said output data, for the purpose of reducing the number of clock cycles required to scan out test results (Wang, page 162, column 2, lines 13-16).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication 2007/0067688, Vranken et al.
U.S. Patent Application Publication 2002/0162066, Khoche et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571)272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dfm
01/18/08

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